

FIG. 1

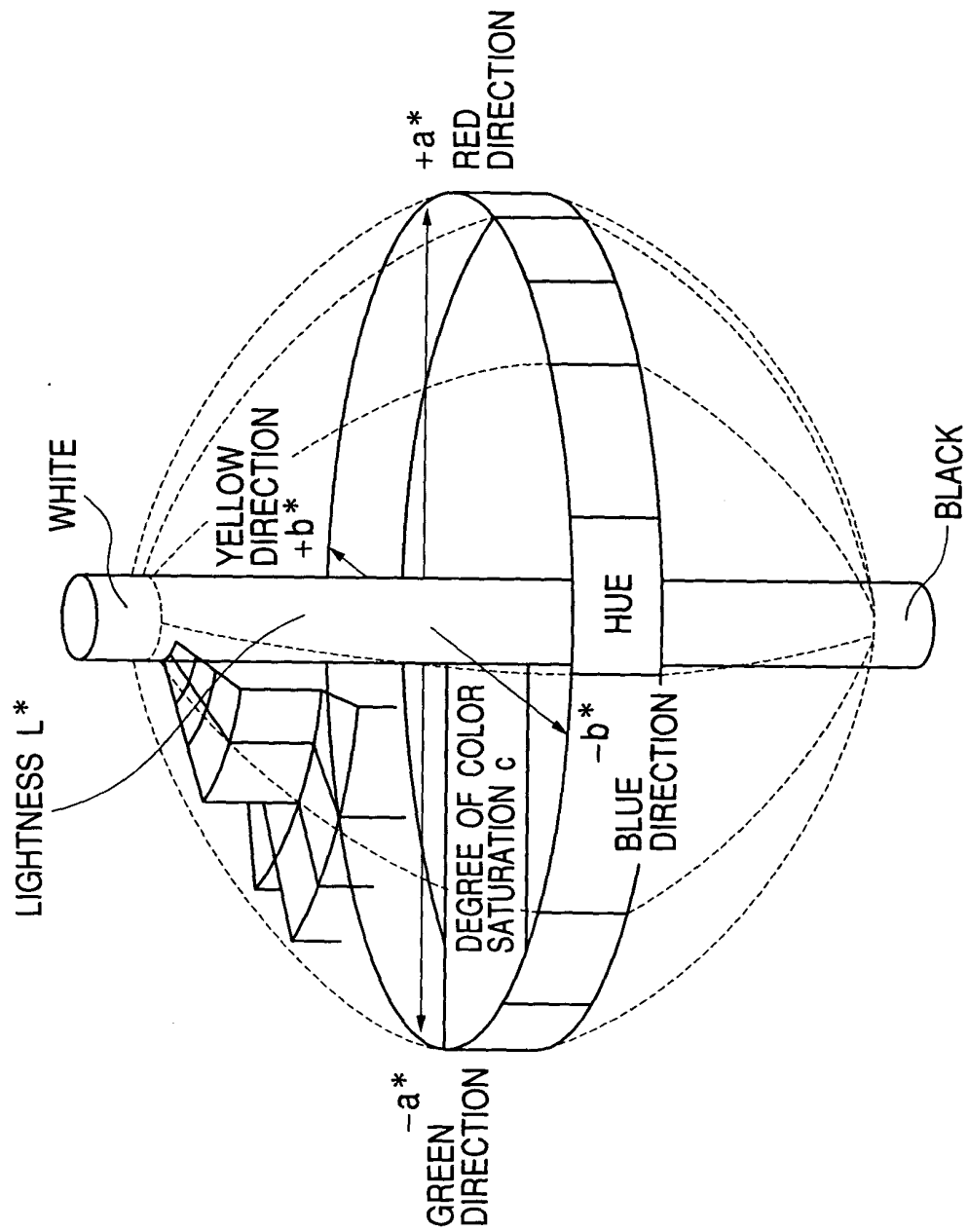


FIG. 2

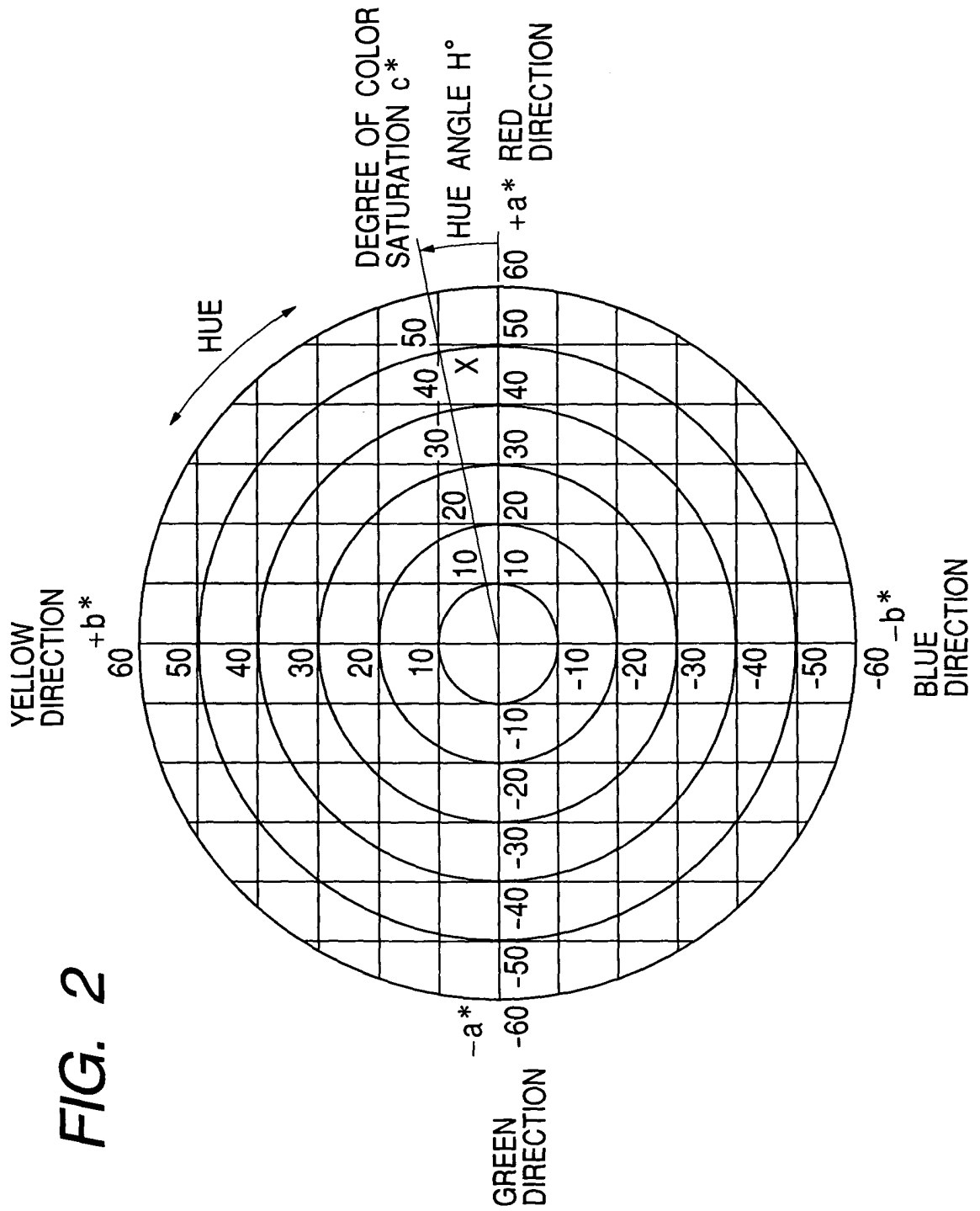


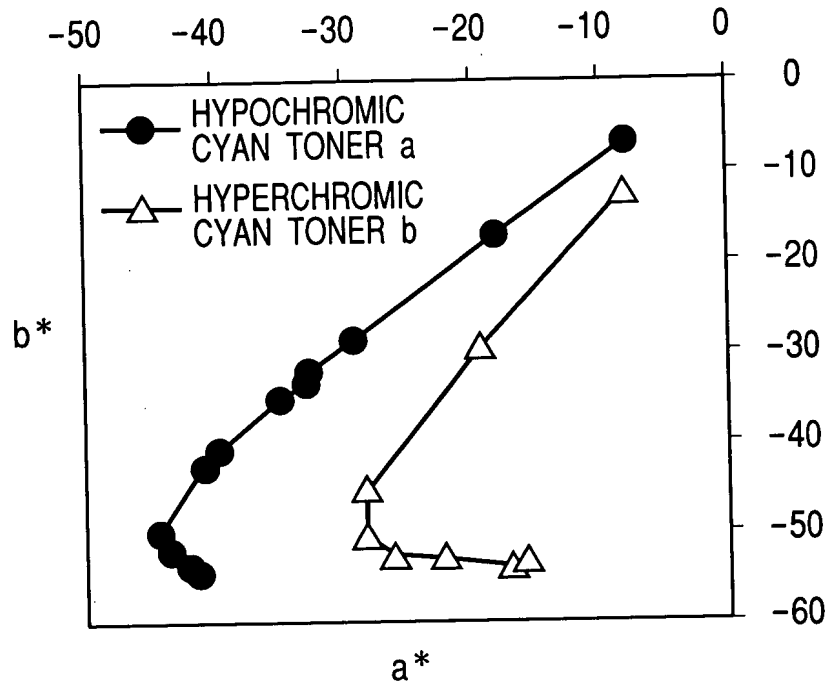
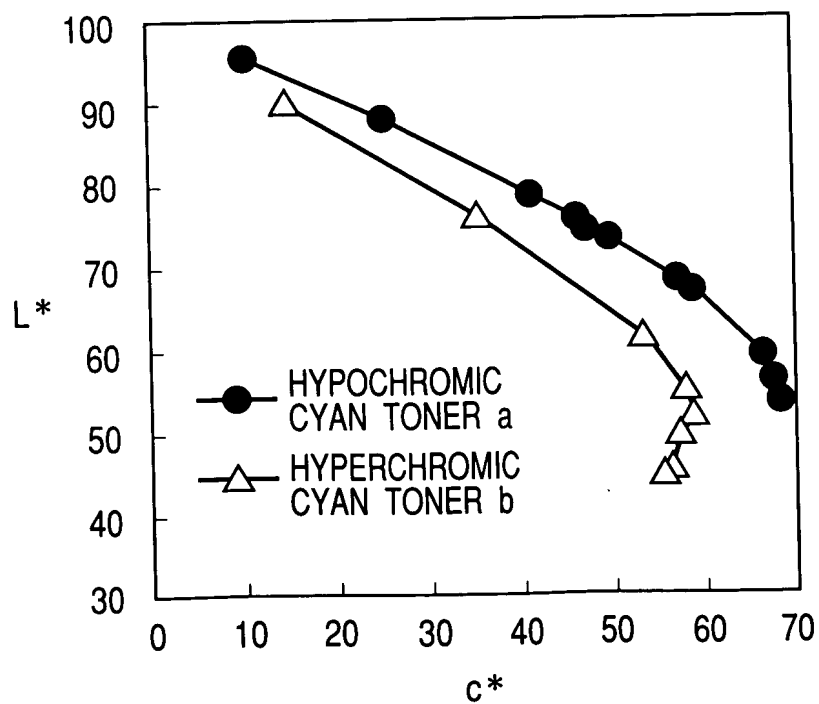
FIG. 3**FIG. 4**

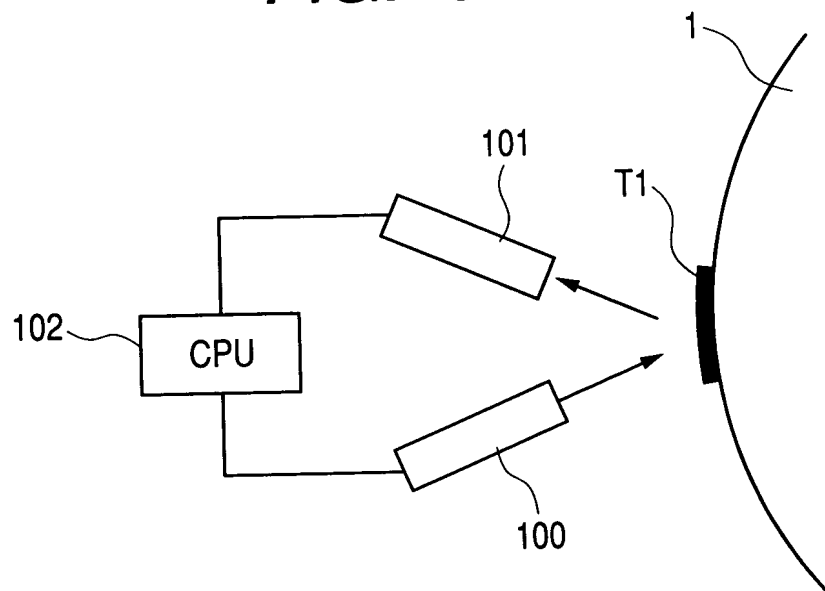
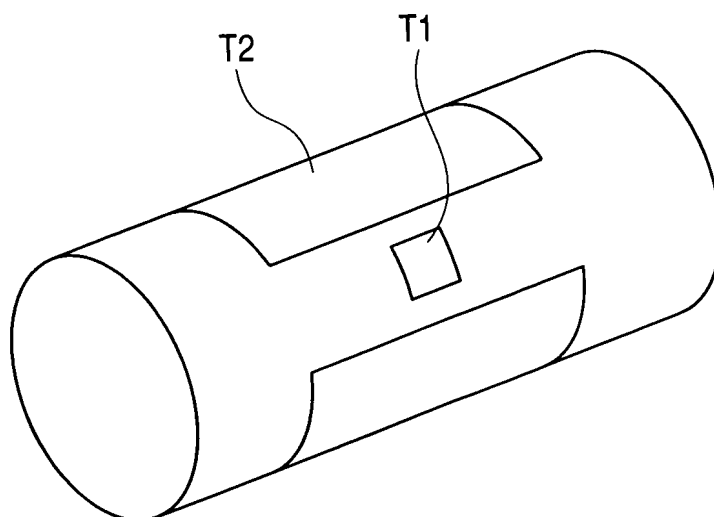
FIG. 5A**FIG. 5B**

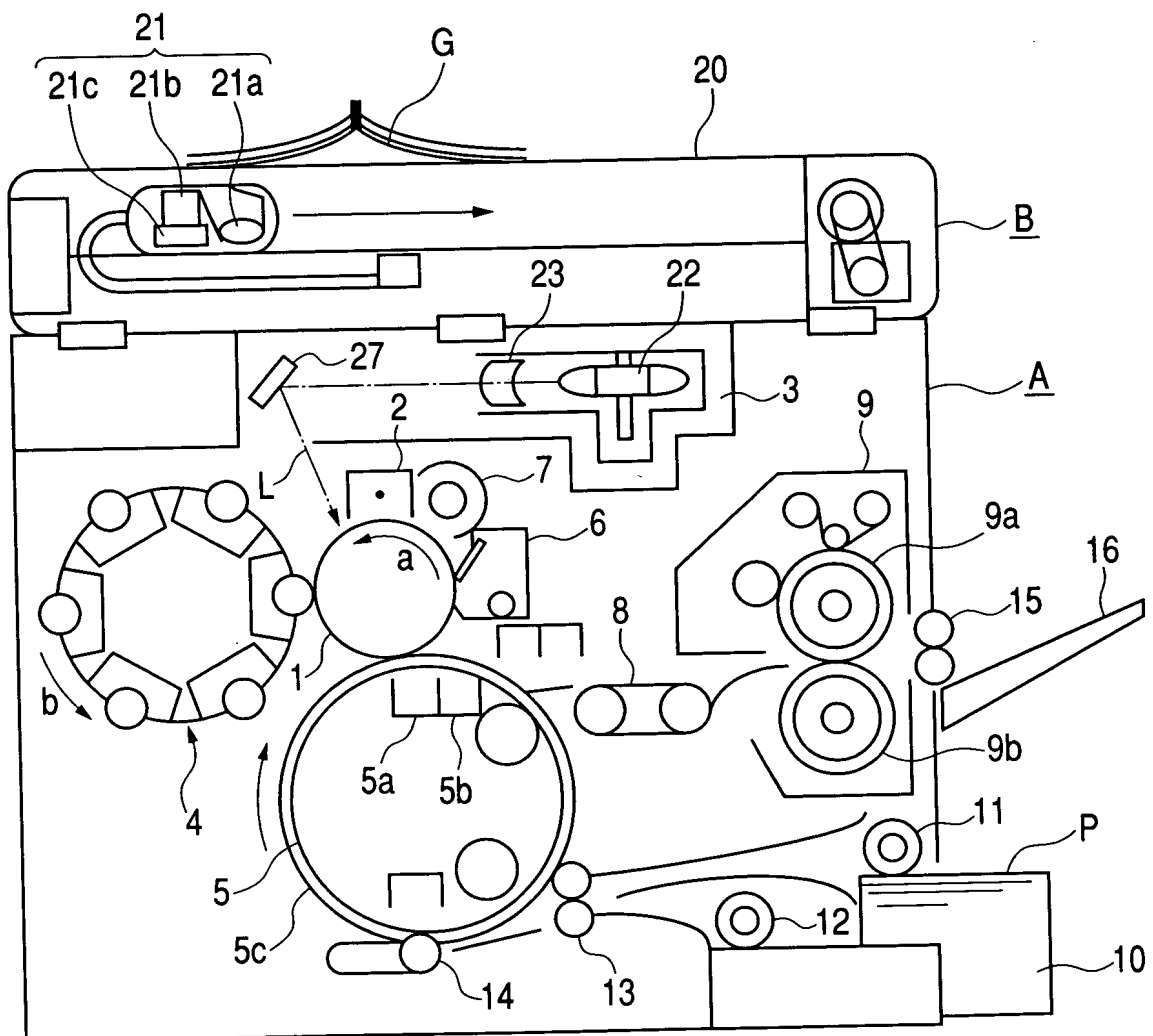
FIG. 6

FIG. 8

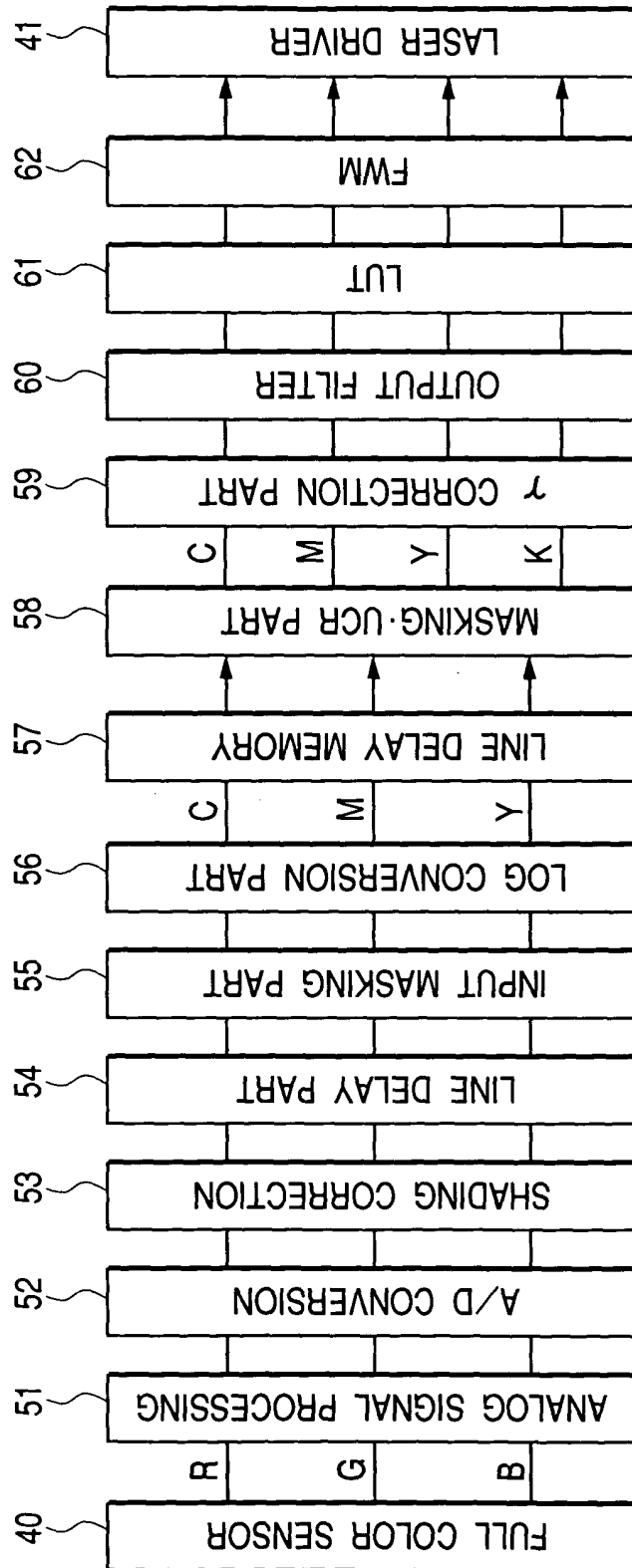


FIG. 9

$$\begin{bmatrix} R_0 \\ G_0 \\ B_0 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \begin{bmatrix} R_i \\ G_i \\ B_i \end{bmatrix} \dots\dots\dots (2)$$

WHERE; R_0, G_0, B_0 OUTPUT SIGNAL
 R_i, G_i, B_i INPUT SIGNAL

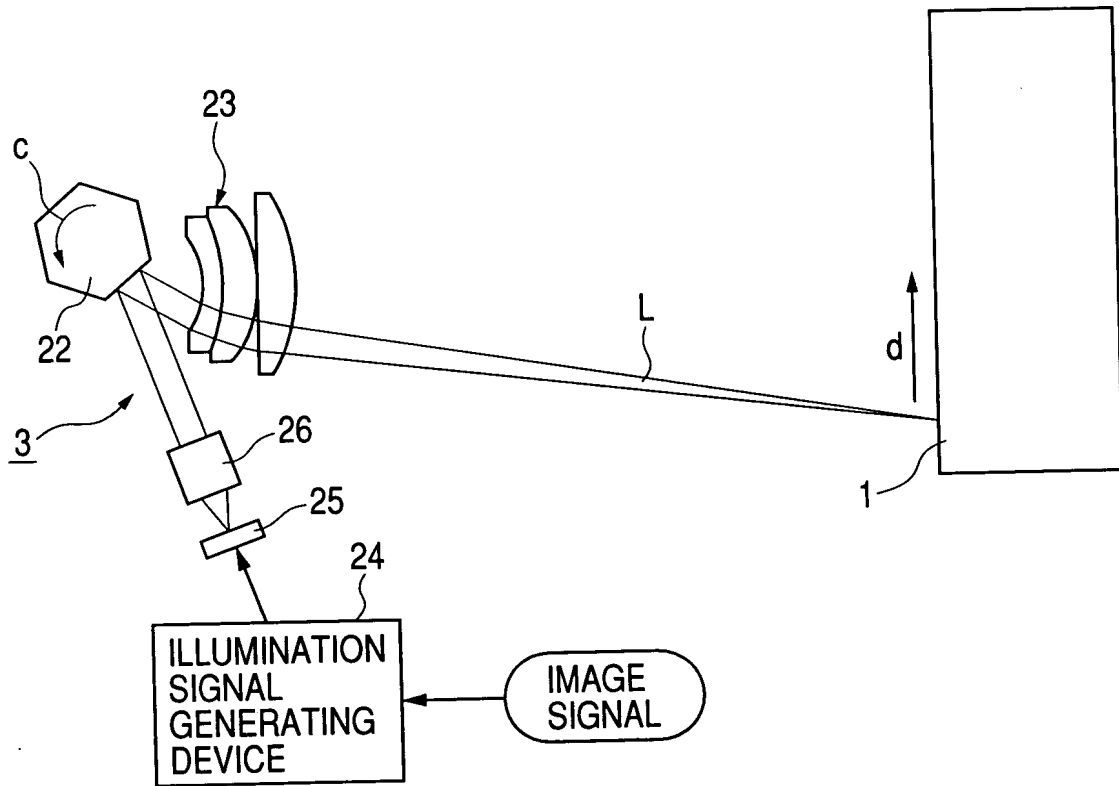
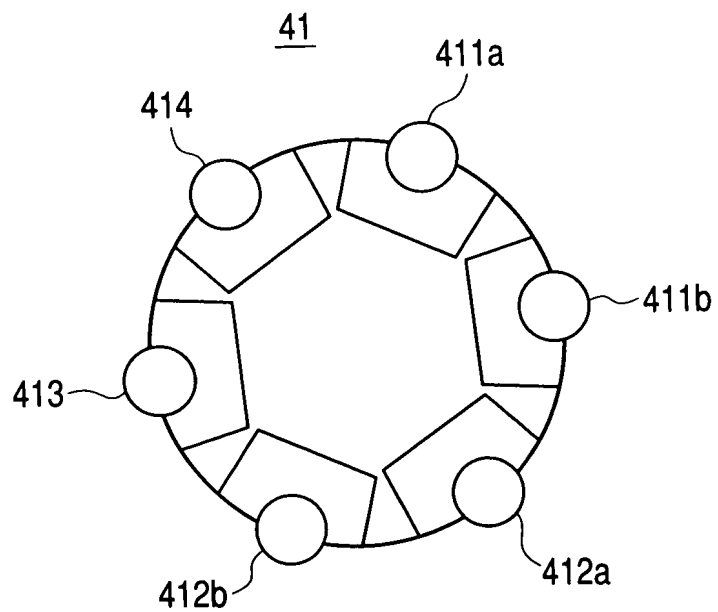
FIG. 10**FIG. 11**

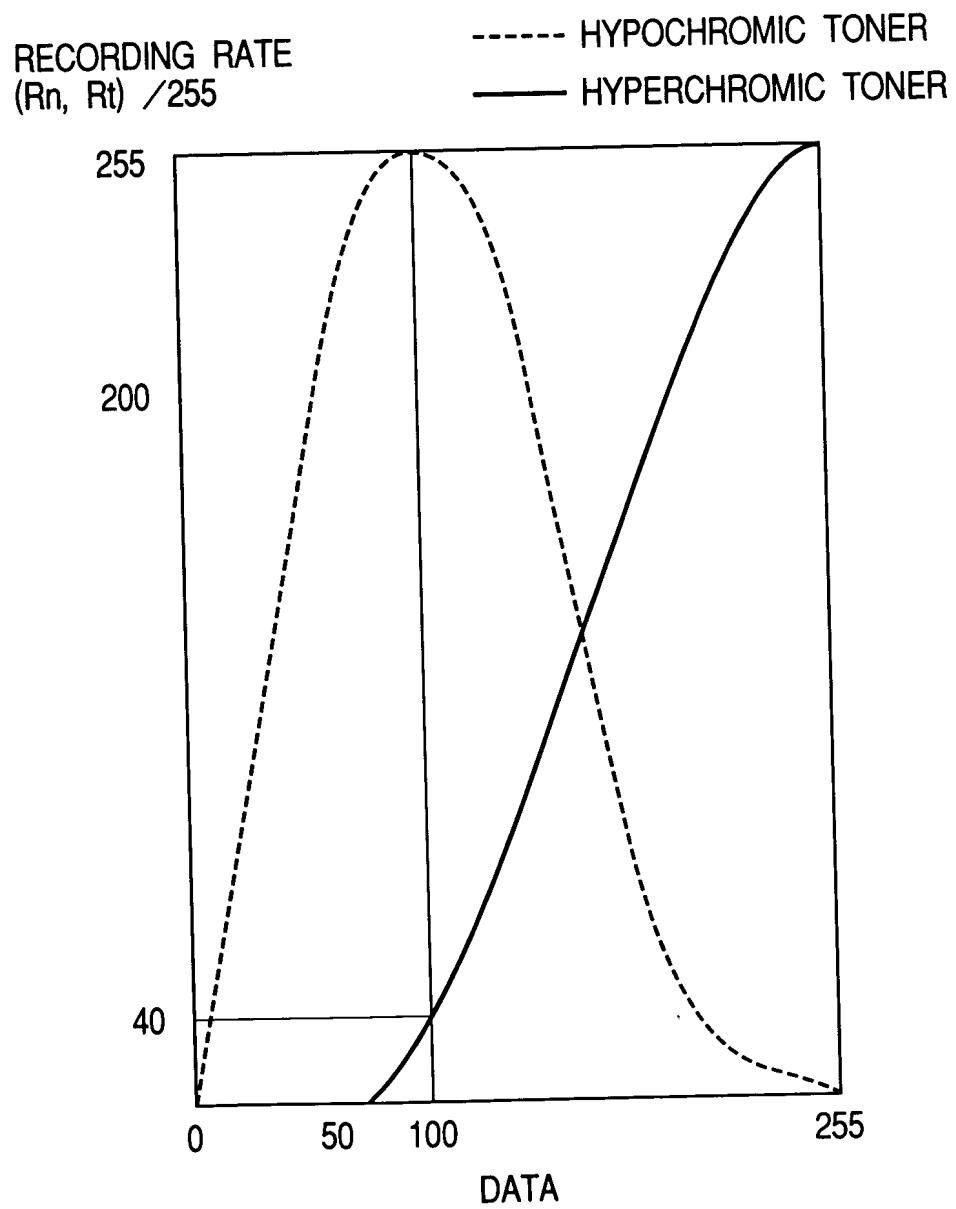
FIG. 12

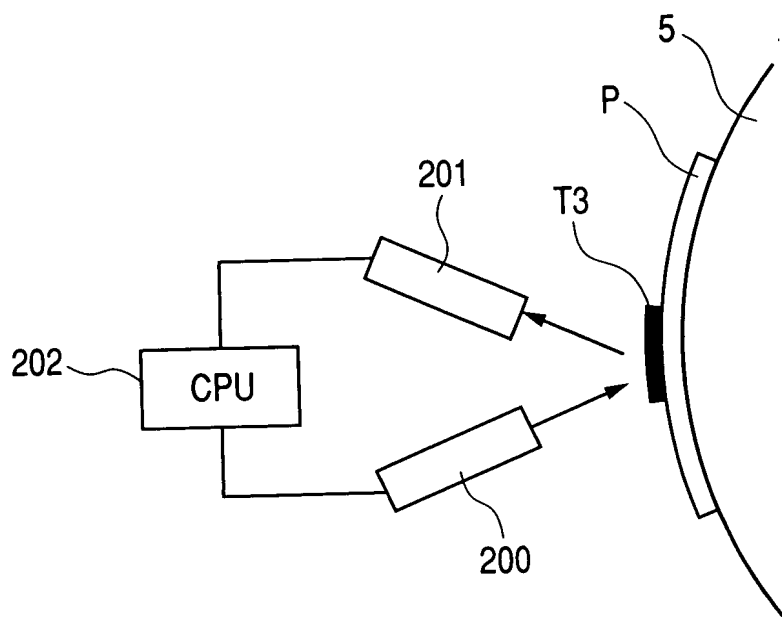
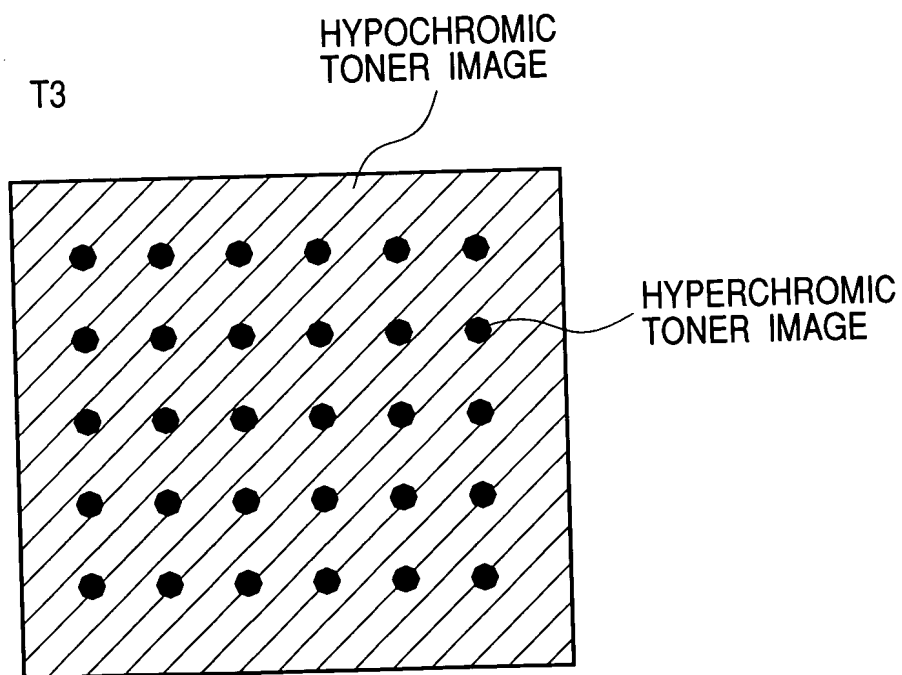
FIG. 13**FIG. 14**

FIG. 15

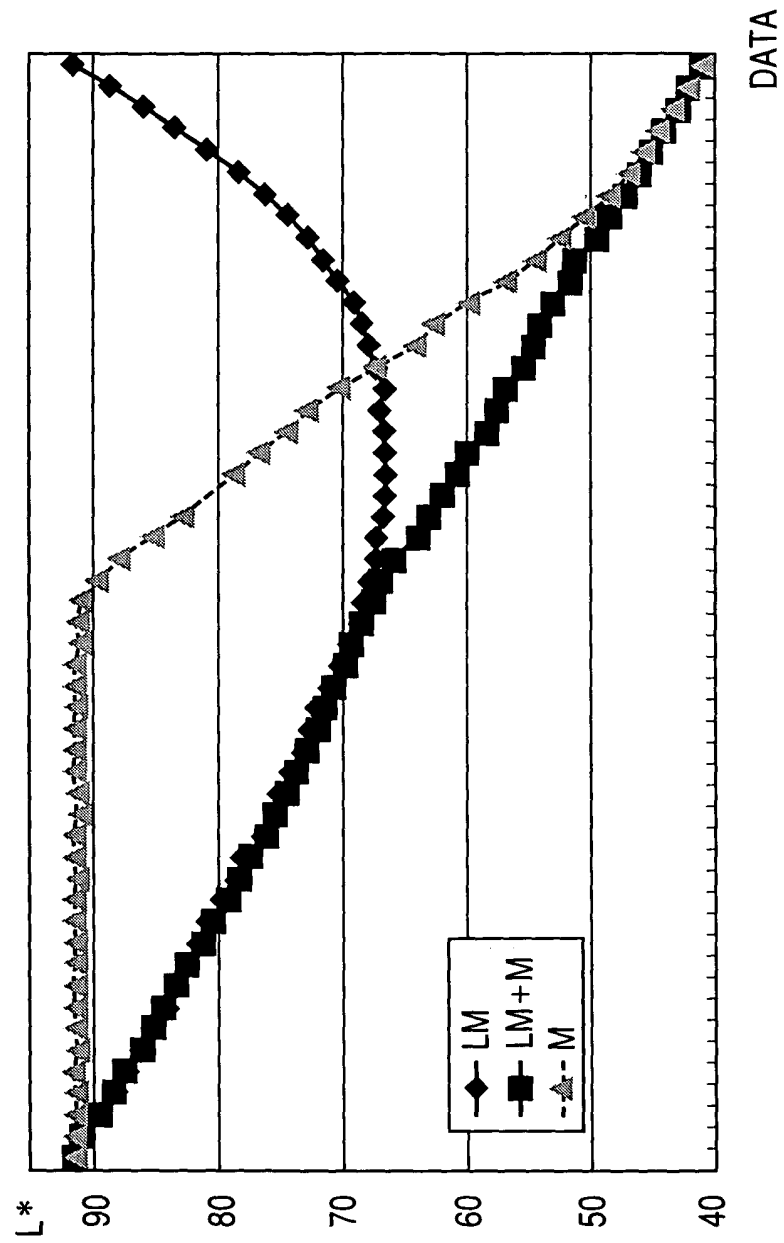


FIG. 16

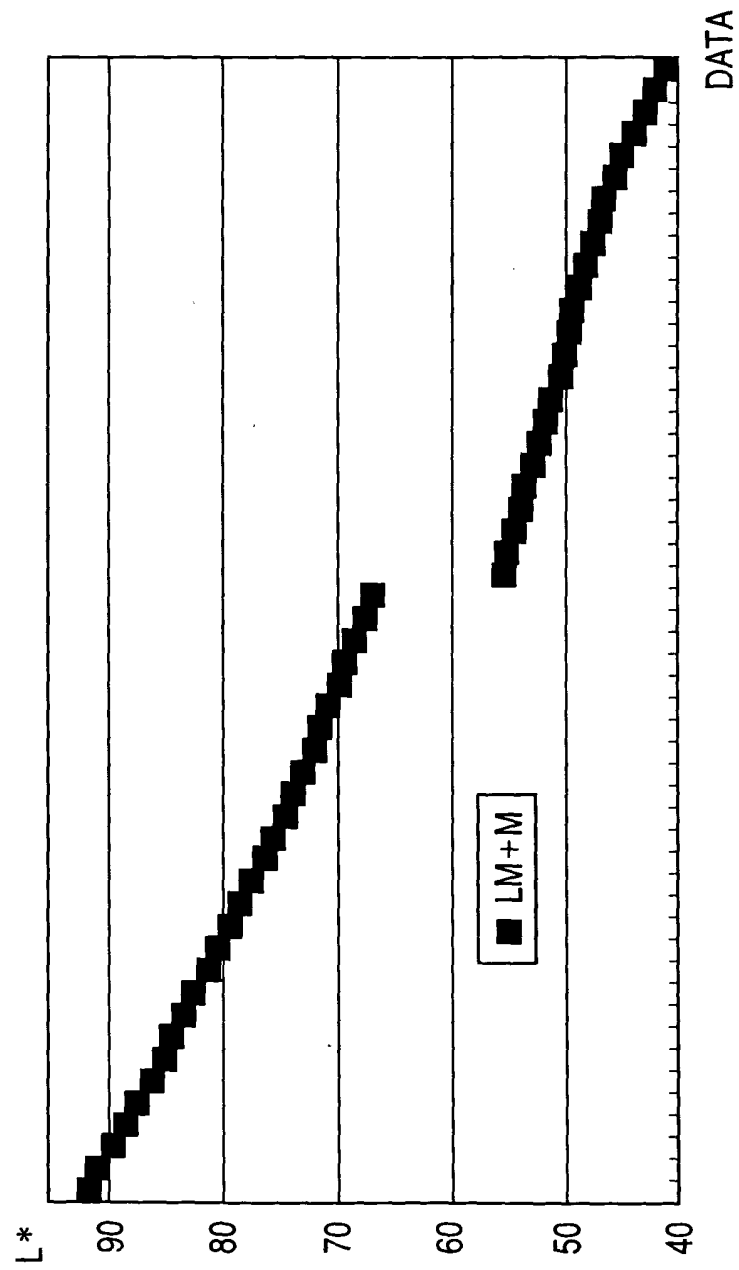


FIG. 17

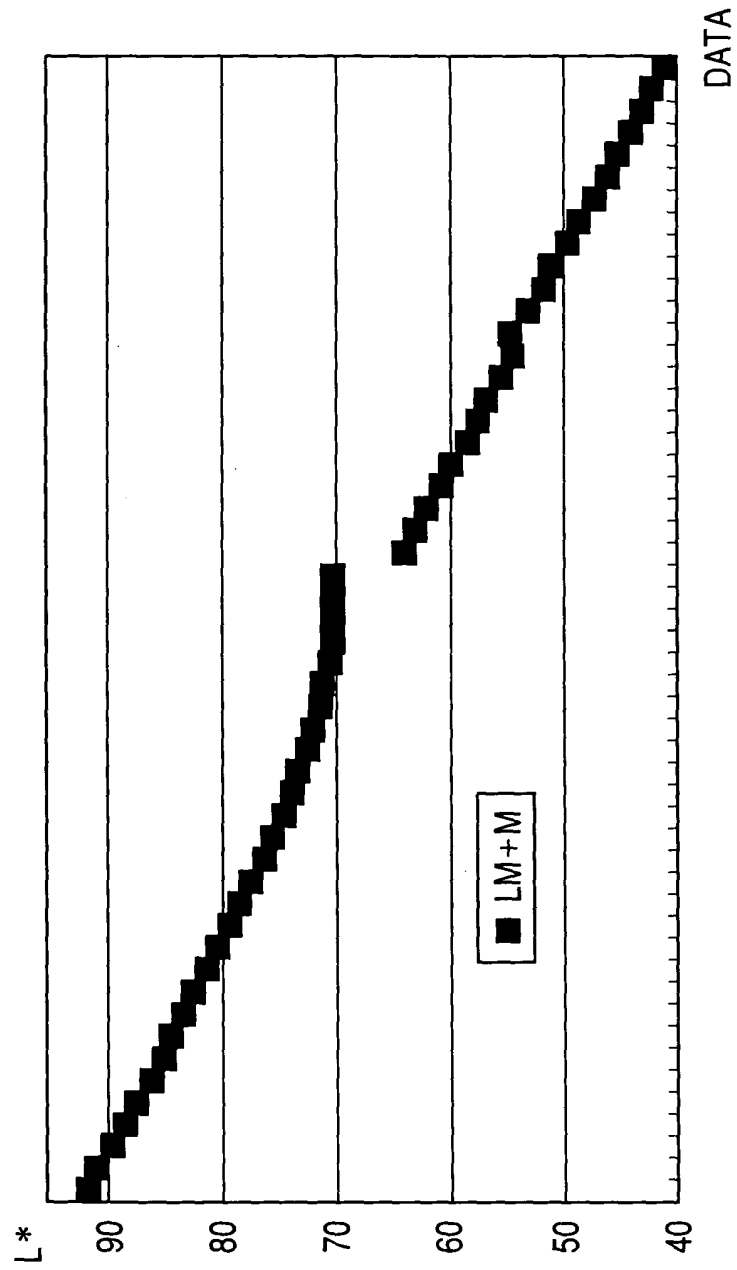


FIG. 18

